NOVELLUS' ULTRA-THIN DIELECTRIC DIFFUSION BARRIERS BOOST 32nm INTERCONNECT PERFORMANCE

San Jose, Calif. - April 1, 2009 - In order to support the RC delay scaling required by the International Technology Roadmap for Semiconductors (ITRS), process designers have focused their attention on reducing the permittivity of dielectrics used in the interconnect stack. Research has shown that significant reduction in the permittivity of the overall interconnect stack can be achieved by focusing on the material properties and deposition method of the dielectric diffusion barrier. Innovative deposition and pre-treatment technologies have been developed using Novellus' (NASDAQ: NVLS) patented multi-station sequential processing (MSSP) architecture to create ultra-thin dielectric barriers that minimize impact on RC delay while ensuring stringent electromigration (EM), dielectric breakdown, and line-to-line leakage requirements are met.

Figure 1 illustrates two options available to a process designer to achieve a 10 percent reduction in effective dielectric constant (k-effective). From a baseline k-effective value of approximately 3.3, using a dielectric barrier with k of 5.0 and a thickness of 50nm, a 10 percent reduction can be achieved either by introducing a new dielectric barrier material with a k of 3.8 or by reducing the thickness of the current dielectric barrier to 25nm. Thinning the dielectric barrier is the less complicated of the two changes, since no new materials are introduced into the integration scheme. However, ultra-thin barriers present their own deposition challenges where hermeticity and copper diffusion resistance need to be maintained at the reduced film thickness. Taking advantage of interface and bulk film controls afforded by MSSP, Novellus researchers have successfully demonstrated dielectric barriers down to 10nm thickness exhibiting the same EM, dielectric breakdown and line-to-line leakage characteristics as 50nm thick films.

Figure 1: Modeled line to line keffective by for various diffusion barrier thicknesses and as deposited k values.

The unique film properties derived from MSSP have led industry-leading manufacturers of logic and memory devices to implement dielectric diffusion barriers fabricated using the Novellus VECTOR® PECVD system. Figure 2 shows a 65nm device cross section with both dielectric diffusion barrier and contact etch stop layers deposited using the MSSP approach.

Figure 2: 65nm device cross section showing diffusion barrier and contact etch stop deposited using MSSP. Image courtesy of Intel.

"The dielectric diffusion barrier is a critical layer in the interconnect stack due to the role it plays in determining device reliability," said Kevin Jennings, senior vice president and general manager of Novellus' PECVD business unit. "Novellus' diffusion barrier films meet today's performance needs and have been demonstrated to meet the EM and dielectric breakdown requirements for future technology generations."

For more information regarding the use of thinned dielectric diffusion barriers to scale RC delay, check out www.NovellusTechNews.com/Thin-Barriers.aspx.

About Novellus' PECVD Technology:
For high-volume manufacturing applications at 45nm and beyond, Novellus' advanced low-k, ILD, IMD, and dielectric diffusion barrier films offer the lowest k-effective, superior RC control, and an easily integrated low-cost dielectric solution.

About Novellus:
Novellus Systems, Inc. (Nasdaq: NVLS) is a leading provider of advanced process equipment for the global

semiconductor industry. The company's products deliver value to customers by providing innovative technology backed by trusted productivity. An S&P 500 company, Novellus is headquartered in San Jose, Calif. with subsidiary offices across the globe. For more information, please visit www.novellus.com

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