Motorola Demonstrates Successful Integration Of Lam Research Corporation's Cmp And Etch Systems For Copper Back-End

Motorola Demonstrates Successful Integration Of Lam Research Corporation's Cmp And Etch Systems For Copper Back-End Fremont, Calif., February 21, 2001 - Lam Research Corporation (Nasdaq: LRCX) today announced that Motorola, Inc.'s (NYSE:MOT) Semiconductor Products Sector, a global leader in the development of copper chip technology, recently completed a successful Copper Dual Inlaid multilevel interconnect demonstration with Lam and Novellus Systems, Inc. (Nasdaq: NVLS). The demonstration was achieved using Lam's advanced 300 mm Teres® Chemical Mechanical Planarization (CMP) system, with Linear Planarization Technology™ (LPT), and 300 mm Dielectric Etch systems. Three critical parameters (contact resistance, sheet resistance, and line to line leakage) were shown to be at the same or better levels as compared to interconnect results on 200 mm.

"This collaboration with Lam and Novellus has been two years in the making and the remarkable performance justifies our efforts," said Doug Keenan of Digital™ Laboratories' APRDL (Advanced Products Research and Development Laboratory) organization at Motorola, Austin, Texas. "We were extremely impressed with the results achieved, demonstrating a path for copper processing to transition to 300 mm."

This work is part of Motorola's strategy for 300 mm equipment development, which is aimed at preparing Motorola to enter 300 mm production with a set of mature, production-ready fabrication technologies. Motorola and Infineon Technologies AG recently completed their joint venture's successful production of saleable devices utilizing 300 mm equipment.

"Lam has enjoyed the opportunity to work with Motorola on this project to demonstrate our world-class capabilities in 300 mm Etch and CMP for dual damascene copper multilevel interconnects," said Nick Bright, Lam's vice president of Technology and Engineering. "The challenge of moving the wafers through multiple supplier sites for a virtual lab effect was impressively managed by Motorola's APRDL team within the Digital™ Laboratories. This effort was further supported by the close relationship Lam has with Novellus through the Damascus Alliance."

"The 300 mm Teres CMP system is a direct scale up of our 200 mm Teres and is capable of processing 200 mm wafers as well, which is a big advantage to customers as they make the transition to the larger wafer size," commented Kevin Crofton, deputy general manager of Lam's CMP/Clean Product Group. "Motorola's evaluation confirms that the scale up design philosophy which Lam has implemented on both Etch and CMP systems enables 200 mm to 300 mm process portability and therefore provides accelerated learning for our customers."

This news release contains certain forward-looking statements, which are subject to the Safe Harbor provisions created by the Private Securities Litigation act of 1995. Such forward-looking statements include, without limitation, the prospective demand for and customer use of the company's products, acceptance and competitiveness of the company's products, future machine and process performance, operating costs in a production environment, and market transition to new products and processes. Such statements are based on current expectations and are subject to risks, uncertainties, and changes in condition and other risks detailed in documents filed with the Securities and Exchange Commission, including specifically the report on Form 10-K for the year ended June 25, 2000, and the Form 10-Q for the quarter ended December 24, 2000. The company undertakes no obligation to update the information in this Press Release.

Lam Research Corporation is a leading supplier of front-end wafer processing equipment and services to the worldwide semiconductor manufacturing industry. The company’s common stock trades on the Nasdaq National Market under the symbol LRCX. Lam’s World Wide Web address is http://www.lamrc.com.

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