COPPER RESISTIVITY FIXABLE FOR 45 NM NODE, BUT LONG-TERM ISSUES REMAIN, SEMATECH AND NOVELLUS WORKSHOP REVEALS

Austin, TX and San Jose, CA (6 July, 2005) - Copper resistivity will remain a challenge for the semiconductor industry, but chip designers are likely to use hierarchical design workarounds to modify the metal for linewidths at the 45 nm technology node, according to participants at an industry workshop sponsored by SEMATECH and Novellus Systems, Inc. (Nasdaq NM: NVLS).

Commenting on the recently concluded Copper Resistivity Workshop in Burlingame, CA, SEMATECH and Novellus interconnect specialists shared insights on results of the recent meeting, which drew approximately 160 engineers. The industry-wide workshop, co-sponsored by SEMATECH and Novellus, focused on ways to extend the use of copper in advanced semiconductors in the face of increasing copper resistivity at linewidths below 90 nm.

"Due to the fundamental laws of physics, copper resistivity is bound to increase and will result in several critical issues that need to be addressed," said Andreas Knorr, conference co-chair and manager of the Advanced Materials Development Program in SEMATECH's Interconnect Division. "Various process refinements could alleviate perhaps 5 to 15 percent of the problem, provided that chip manufacturers are willing to accept added cost and design complexity."

Below 90 nm linewidths, copper resistivity rises dramatically because of increased electron scattering on grain boundaries and interfaces. These resistivity increases can sharply diminish or wipe out the capacitance benefits of low-k dielectric materials, which have long been an industry focus.

"The increase in resistivity of an ultrathin wire was of academic interest long before the first IC", said Ron Powell, conference co-chair and Novellus fellow. "But we have been so successful at scaling down CMOS devices and wiring that we now have to consider the practical impacts of these 'size effects' as well."

"Ironically, the switch from aluminum to copper wiring has accelerated the problem, since size effects show up in copper at closer-in technology nodes. Regardless of how the situation came about, it is likely to be addressed by a synergistic combination of materials, process and design changes," Powell added. "Novellus and SEMATECH therefore conceived of a cross-functional workshop to raise awareness of the problem and drive a solution."

At the resistivity workshop, experts sought to build consensus on the contributions and root causes of metal line resistivity increases at wire widths below 90 nm, discuss the performance and reliability impact of these surges and consider potential solutions with innovative approaches to materials, process and integration, and circuit design. Industry analyst Dan Hutcheson of VLSI Research praised the conference as "truly problem focused," adding that it was "chock full of ideas with lots of theoretical detail to understand the mechanisms backed up with real research into potential solutions."

Knorr and Powell said the workshop highlighted two promising "process fixes" that could moderately mitigate the effects of resistivity:

- Minimize the volume that diffusion barriers occupy by making them ultra-thin
- Enlarge copper grains to diminish boundaries and encourage unimpeded electron flow.

While participants believed that designers using hierarchical design rules will be able to work around the resistivity increase to reach the 45 nm node, they warned that it will be critical to minimize line resistance differences induced by process variation. These differences originate mostly with lack of adequate critical dimension (CD) control and dishing and erosion problems caused by chemical mechanical polishing (CMP), resulting in line cross-section variations. Also, workshop experts cautioned that reliability in fine lines will be a critical issue due to generally smaller grain sizes, and higher ratios of metal surface area to metal volume.

"The ultimate solutions will probably come in the form of short lines and a move to three-dimensional interconnect," said Sitaram Arkalgud, SEMATECH's Interconnect director. But he added that despite copper's inherent problems, the workshop revealed scant support for returning to the metal it replaced several years ago.

"The entire audience was asked if they planned to move back to aluminum, and the answer was a resounding 'No,' " Arkalgud recalled. "Only one person suggested that it was even a possibility."

Arkalgud said SEMATECH will continue to guide member companies and the industry in seeking effective resistivity solutions for the subsequent 32 nm and 22 nm technology nodes, including exploration of shorter lines 3D architecture. "Effective interconnect is vital to remaining on the Roadmap, and we'll be exploring a variety of options to make sure we can offer effective solutions at the right time," Arkalgud said.

Glenn Alers, principal engineer at the Novellus Customer Integration Center, said: "Novellus will continue to work with university groups to generate fundamental understanding of scattering mechanisms at copper interfaces, to model the impact of size effects on overall interconnect performance, and to stimulate out-of-the-box solutions. We will also be driving new processes into the industry that, among their other benefits, will reduce effective copper resistivity. For example, expect to see more use of ultrathin diffusion barriers deposited by ion induced atomic layer deposition (i-ALD) to maximize copper volume, and electrodeposition chemistries and annealing procedures to produce large copper grains in narrow trenches."

"Safe Harbor" Statement Under the Private Securities Litigation Reform Act of 1995:

The statements regarding (i) the ongoing challenge presented by copper resistivity and likely design workarounds; (ii) the use of synergistic materials, process and design changes to address "size effects"; (iii) the ability to mitigate resistivity by minimizing volume occupied by diffusion barriers and enlarging copper grains; (iv) the use of hierarchical design rules to reach the 45 nm node; (v) short lines and three-dimensional interconnect as a solution to resistivity; (vi) Novellus' commitment to work with university groups to increase understanding of scattering mechanisms, to model "size effects" and stimulate solutions; and (vii) expected use of ultrathin diffusion barriers and electrodeposition chemistries and annealing procedures; that are not purely historical data, are forward-looking statements. The forward-looking statements involve risks and uncertainties, including, but not limited to, the inability to solve resistivity challenges through and technical difficulties with design workarounds, synergistic solutions, minimizing diffusing barriers or enlarging copper grains; Novellus' inability to generate solutions from scattering mechanisms or "size effects" models; and unanticipated difficulties precluding the use of ultrathin diffusion barriers and electrodeposition chemistries, as well as other risks indicated in our filings with the Securities and Exchange Commission (SEC). Actual results could differ materially. We do not assume, and expressly disclaim, any obligation to update this information. For more details, please refer to our SEC filings, including our Annual Report on Form 10-K for the year ended December 31, 2004, our Quarterly Report on Form 10-Q for the quarter ended April 2, 2005, and our Current Reports on Form 8-K filed or furnished April 7, 2005, April 18, 2005, April 29, 2005, and May 5, 2005.

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