PETER WOLTERS' INNOVATIVE SILICON WAFER GRINDING TECHNOLOGY PRODUCES 5X FLATTER WAFERS

PPG Process Delivers Global and Local Flatness Values That Exceed 22nm Requirements

RENDSBURG, Germany - March 31, 2010 - Peter Wolters GmbH, a leading manufacturer of high-precision machine tools and a wholly owned subsidiary of Novellus Systems (NASDAQ: NVLS) today announced that it has developed innovative Planetary Pad Grinding (PPG™) technology based on the well-established AC2000 platform's double-sided processing architecture. The PPG technology produces prime silicon wafers that are five times flatter than those achieved using other grinding techniques, and it reduces defect levels by 3X for next-generation device nodes as compared to conventional lapping processes.

Shrinking device dimensions and advanced lithography wavelengths are driving tighter wafer flatness and defectivity specifications for the prime silicon wafers used in the semiconductor manufacturing process. One of the steps used to convert raw silicon into prime wafers involves the removal of a lower-quality crystalline surface layer caused by the silicon ingot sawing step. Until now, lapping or high-speed cup-wheel grinding was used to remove this inferior crystalline layer. However, both methods have distinct disadvantages due to surface abrasion and flatness issues. Lapping causes relatively severe defects to propagate through the silicon wafer surface, extending into the crystal structure by more than 20 microns. Cup-wheel grinding is limited by the ultimate flatness levels that can be obtained, since the curved contact zone between the grinding wheel and the wafer creates a well-known spiral surface pattern with an undesirable center mark. Both the defect and flatness issues limit the use of the lapping and cup-wheel grinding approaches for 32nm technology and beyond.

Silicon wafer polishing technology has used planetary motion for some time to produce ultra-flat wafers during the double-sided polishing process that follows the grinding step. However, transferring this technology to the grinding step has been problematic.

Peter Wolters' engineers have developed a new silicon wafer grinding technology called PPG that provides industry-leading flatness and defectivity values. Based on the proven AC2000 platform's planetary wafer motion and double-sided processing architecture, fixed-abrasive type grinding pads are used to simultaneously process both sides of the wafer. The Peter Wolters PPG technology - coupled with the company's patented Upper Platen Adaptive Control (UPAC™) - eliminates the problems and limitations of conventional lapping and cup-wheel grinding processes. This innovative processing approach yields silicon wafers with global flatness values (GBIR) down to 500nm and local flatness values (SFQR) down to 100nm, exceeding requirements for the 22nm technology node. The resulting wafers are up to five times flatter than what's achievable with alternative wafer grinding approaches, and have a 3X reduction in defect levels as compared to conventional lapping processes.

An added benefit of this unique grinding technology is the ability to yield more wafer slices per silicon ingot. Peter Wolters' PPG technology removes less silicon during the grinding process due to a significant reduction in sub-surface silicon damage (vs. lapping) and better flatness control (vs. cup-wheel grinding). Since less silicon is removed during the PPG grinding step, the starting wafer slices can be thinner, resulting in up to 20 additional 300mm raw wafers from a 2000mm-long ingot.

"Peter Wolters' new Planetary Pad Grinding technology is well-suited to the new requirements for the extremely flat wafers used for 32nm manufacturing and beyond," said Kay Petersen, Novellus Systems' EVP and general manager of the company's Industrial Applications Group. "The combination of PPG technology with UPAC process control on the AC2000 platform allows us to deliver the best of both worlds: superior surface flatness with low silicon damage."

About Peter Wolters:
Peter Wolters GmbH, a component of Novellus' Industrial Applications group, is a leading manufacturer of high precision surface polishing systems for substrates made of silicon, sapphire, gallium arsenide, silicon carbide and other materials used in the manufacturing of microelectronic, micro-optical, and micromechanical devices. Peter Wolters is headquartered in Rendsburg, Germany. For more information, please visit www.peter-wolters.com.

About Novellus:
Novellus Systems, Inc. (NASDAQ: NVLS) is a leading provider of advanced process equipment for the global semiconductor industry. An S&P 500 company, Novellus is headquartered in San Jose, Calif. with subsidiary offices across the globe. For more information, please visit http://www.novellus.com/technews.aspx.

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