Novellus Announces New Suite of Products For The Advanced Wafer Level Packaging Market

VECTOR® 3D, INOVA® 3D, and G3D™ Models Complement Recently-announced SABRE® 3D System

San Jose, California - July 12, 2010 - Novellus Systems (NASDAQ: NVLS) today introduced new models of the company's VECTOR PECVD, INOVA PVD, and GxT photoresist strip systems. The new models leverage Novellus' advanced interconnect technology to address the evolving requirements of the wafer level packaging (WLP) market. In order to meet the technical challenges of 3D integration, each of these systems incorporates capabilities previously unavailable in conventional packaging equipment, while concurrently delivering industry-leading productivity.

Consumer demand for smaller, more powerful mobile electronics, as well as faster logic and memory chips, is driving the development of alternate packaging technologies that reduce power consumption, increase system-in-package performance, and shrink the form factor. Compared to conventional die packaging, 3D integration technologies like through-silicon vias (TSV) and WLP stacking schemes enable shorter chip-to-chip interconnections that lead to significant performance gains. TSVs allow multiple chips to be stacked vertically in a "sandwich-like" structure and interconnected across very short distances with cross-device copper vias. WLP technologies such as micro-bumps, pillars and copper redistribution layers (RDL) enable increasing I/O counts and decreasing pitch requirements. All of these 3D integration schemes are driving new metal and dielectric interconnect materials and applications.

Novellus has leveraged its interconnect technology leadership to develop a new suite of products that meet both the technological needs and the manufacturing cost constraints of the wafer level packaging market. The newly-introduced SABRE 3D system incorporates state-of-the-art SABRE Electrofill® technology and sets a new industry benchmark for performance and cost-effectiveness. This innovative system includes new, patented technologies like Advanced Pretreatment Technology (APT™) for void-free filling, XMM™ for reduced copper overburden, and TurboCell™ technology for improved fill uniformity at higher throughputs. SABRE 3D's modular architecture can be configured with multiple plating and pre-or-post-treatment cells for a variety of packaging applications including TSV, pillar, RDL, under-bump metallization, and eutectic and lead-free micro-bumping using materials such as copper, tin, nickel, and tin silver.

The INOVA 3D PVD system uses Novellus' next-generation patented HCM® sputtering source coupled with the company's IONFLO™ technology to provide superior copper sidewall coverage and ultra-low defects in high aspect ratio TSVs. The ion-induced copper flow process enables void-free fill to be achieved while using a much thinner seed layer as compared to competitive PVD approaches. This reduces the manufacturing cost of consumables for the TSV PVD process step by greater than 50 percent. INOVA 3D also offers IONX™ titanium and IONX™ XL tantalum source technology that extends target life to greater than 10,000 kW-hrs, resulting in increased uptime and further reducing the overall cost of consumables for this application.

The VECTOR 3D system utilizes the same patented multi-station sequential deposition (MSSD) technology incorporated into more than 1000 VECTOR PECVD tools worldwide. The MSSD architecture, coupled with newly-developed PECVD processes, enables VECTOR 3D to deposit low-cost, low-temperature films that are compatible with bonded substrates. Low-temperature applications include silicon nitride diffusion barriers and silicon oxide isolation and passivation layers. The system incorporates technology to tune the hermiticity and electrical performance of these layers to match the film quality typically obtained with a higher temperature dielectric deposition. VECTOR 3D is also designed for depositing high quality dielectric liners for TSV structures used in both via-middle and via-last integration schemes.

The G3D photoresist strip system has been designed to quickly remove thick (20-100 micron) photoresists used in the manufacture of RDLs and pillars and to achieve residue-free strip and clean of high aspect ratio TSVs. G3D's competitive edge comes from a unique combination of high productivity, low temperature processing, and a deep cleaning capability that's enabled by the system's high ash rate inductively-coupled plasma (ICP) source. The ICP source provides ultra-uniform plasma for consistent resist removal and elimination of post-strip residue. With flexible RF power and gas distribution controls, and a low temperature processing capability, the G3D affords a wide process window for residue-free removal at industry-leading throughputs.

"Wafer level packaging is driving new technology requirements that leverage Novellus' core interconnect competencies in ECD, PECVD, PVD, and photoresist strip," said Dr. Fusen Chen, executive vice president, semiconductor system products. "We have developed a suite of products and applications that apply our advanced deposition and strip technology to the new demands of 3D integration."

About Novellus:
Novellus Systems, Inc. (NASDAQ: NVLS) is a leading provider of advanced process equipment for the global semiconductor industry. An S&P 500 company, Novellus is headquartered in San Jose, Calif. with subsidiary offices across the globe. For more

information, please visit www.novellustechnews.com

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